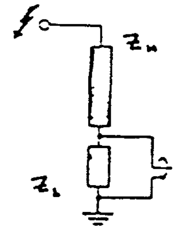
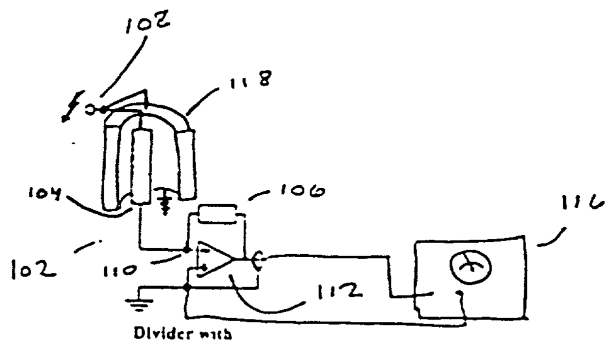


Unbuffered divider.

FIGURE 1



Divider with current receiver.

FIGURE 2

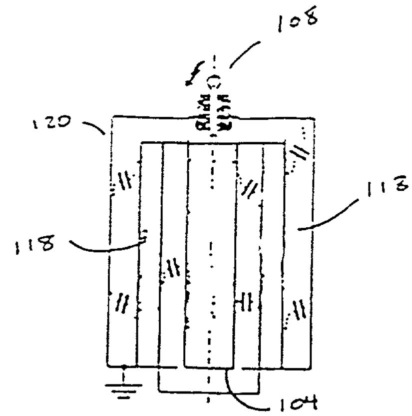


FIGURE 3

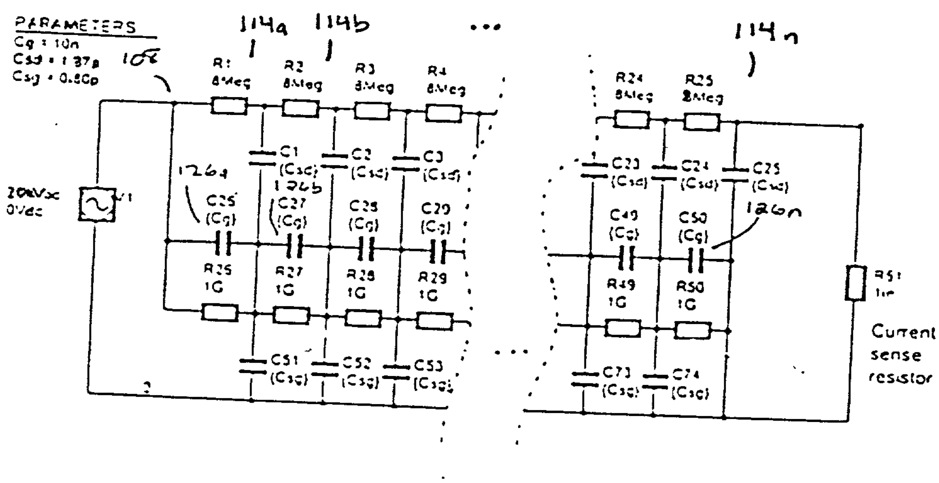


FIGURE 4

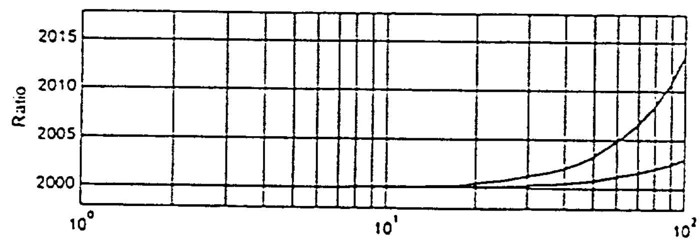


FIGURE 5

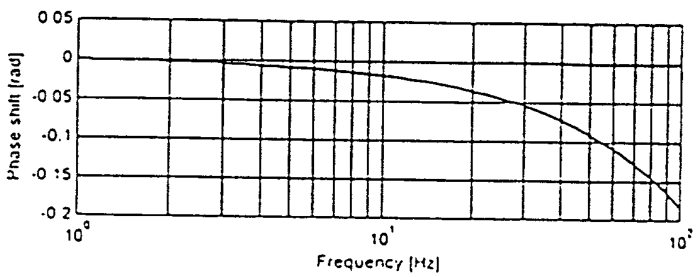
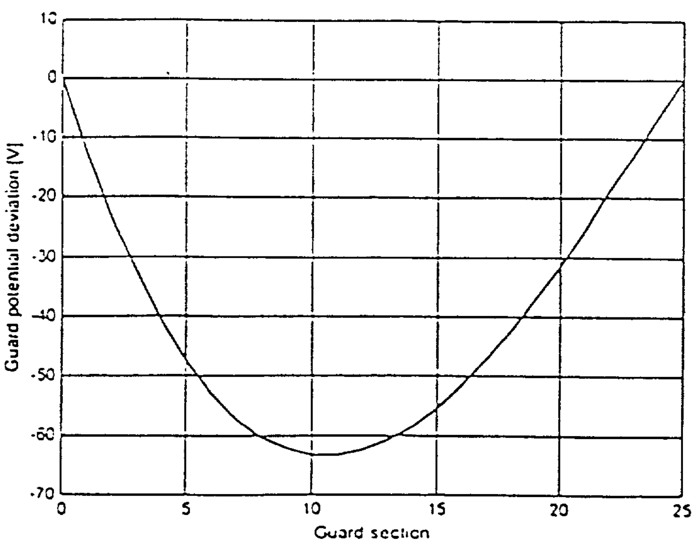


FIGURE 6



Deviation of the guard potential from ideal potential.

FIGURE 7

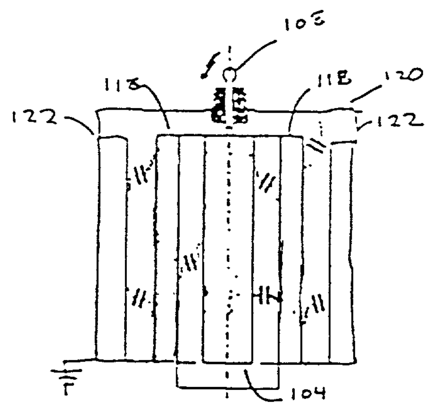


FIGURE 8

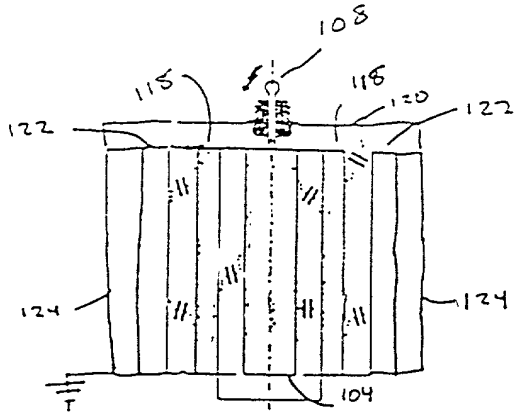


FIGURE 9

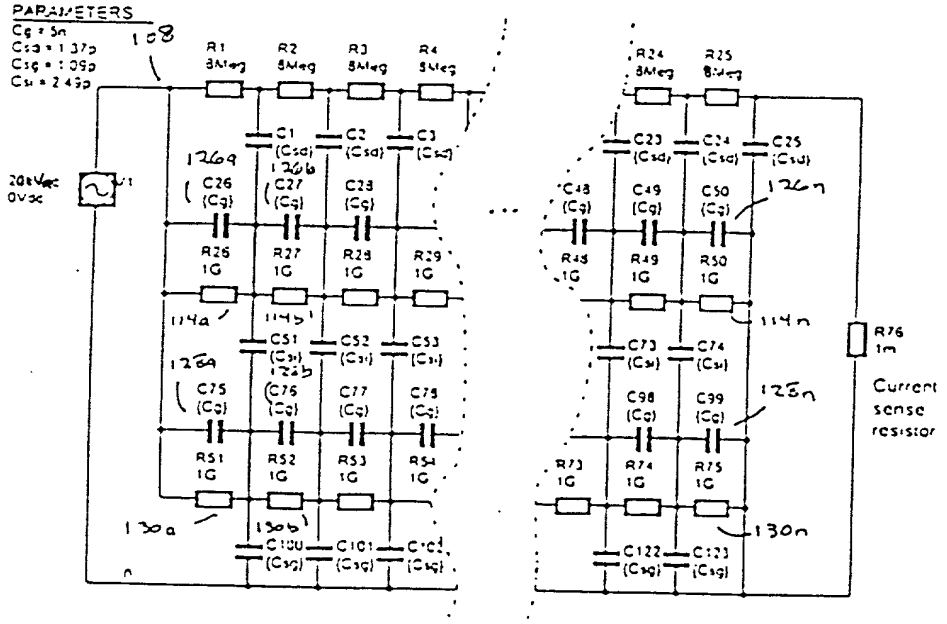
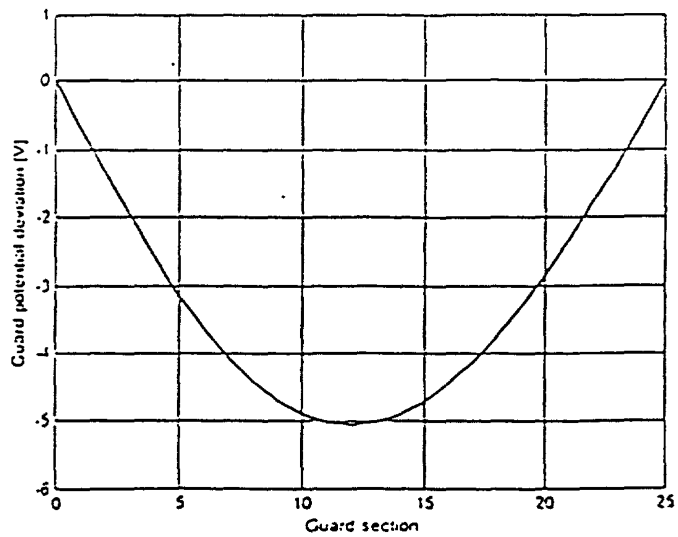
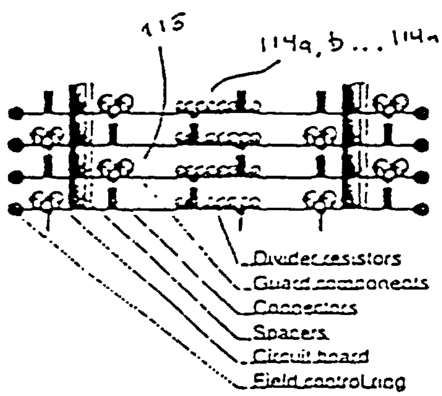


FIGURE 10



Deviation of the inner guard potential from ideal potential.

FIGURE 11



Cross-sectional view of four circuit boards in a divider stack.

FIGURE 12

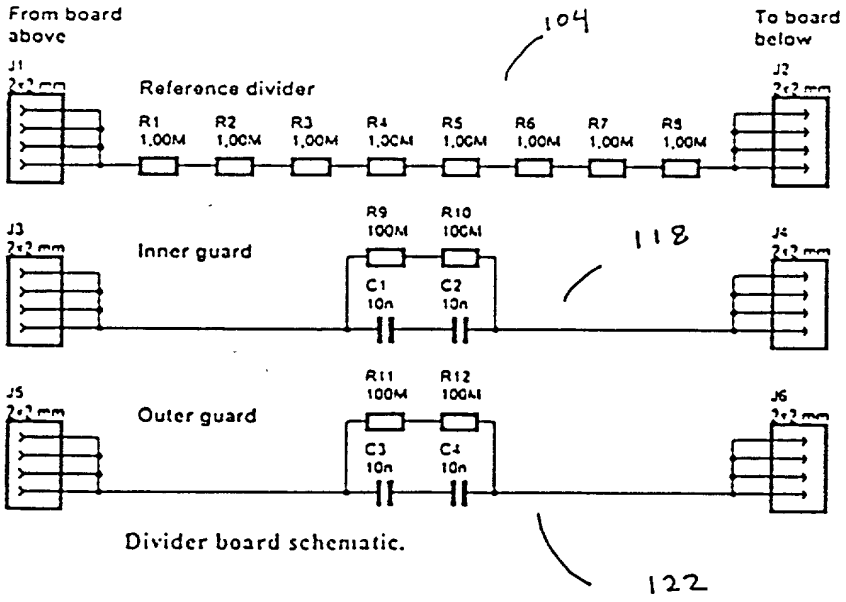

From board above
104
To board below
J1
Reference divider
J2
R1 1.00M
R2 1.00M
R3 1.00M
R4 1.00M
R5 1.00M
R6 1.00M
R7 1.00M
R8 1.00M
J3
Inner guard
R9 100M
R10 100M
C1 10n
C2 10n
118
J4
J5
Outer guard
R11 100M
R12 100M
C3 10n
C4 10n
J6
Divider board schematic.
122

FIGURE 13

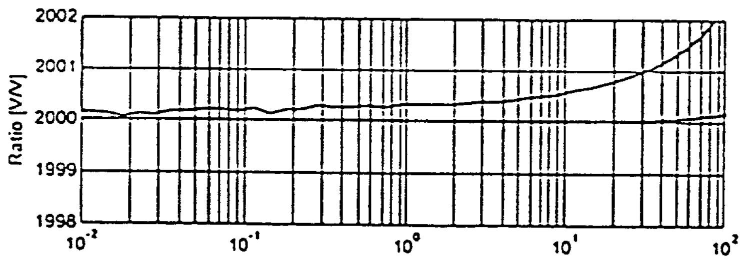


FIGURE 14

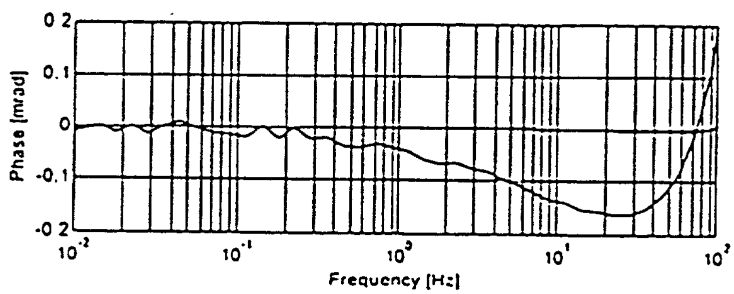


FIGURE 15

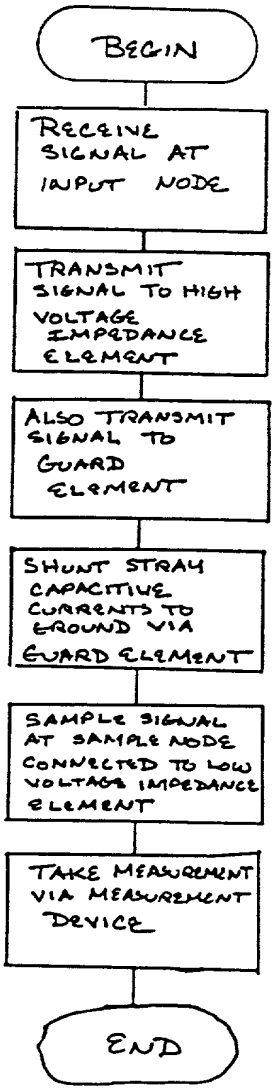


FIGURE 16